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High performance silicene nanoribbon field effect transistors with current saturation

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Abstract. We investigate field effect transistors (FETs) based on semiconducting armchair-edged silicene nanoribbons (ASiNRs) by using ab initio quantum transport calculations. These FETs have high performance with an $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of over 10^6 and a subthreshold swing as small as 90 mV/decade. Impressively, the output characteristic shows a saturation behavior. The drain-current saturation is an advantage with respect to device speed, but it's usually absent in carbon-based (e.g., graphene, graphene nanoribbons, carbon nanotubes, and organic single-molecule) FETs.

1 Introduction

Silicon metal-oxide-semiconductor field effect transistors (MOSFETs) are the building blocks of the modern electronics, and the rapid evolution of modern information society demands higher device performance (e.g., high $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, quick respond, and lower-power consumption). Scaling down the MOSFETs is a significant key to improve the device performance [1,2]. Nowadays, processors containing two billion MOSFETs (gate length ≈30 nm) are in mass production [3]. However, it is a consensus that MOSFET scaling down is approaching its limits because field effect transistors (FETs) with short gates frequently suffer from short-channel effects, such as threshold voltage roll-off, drain-induced barrier lowering, and impaired drain-current saturation [2,4]. Scaling theory predicts that reducing the thickness of the gate insulator and the semiconductor body can make the FETs be robust against short-channel effects down to very short gate lengths [5]. Therefore, monolayer materials such as graphene are highly appreciated.

Very recently, the synthesis of epitaxial single-layer silicene sheets on Ag(111) substrate [6] has been proved through the combination of scanning tunneling microscopy (STM), angular-resolved photoemission spectroscopy (ARPES), and the calculations based on density functional theory (DFT) and tight-binding (TB) approximation. For example, the average Si-Si distance obtain from STM images is 0.22 nm (±0.01 nm) [6], in excellent agreement with the DFT values of 0.225 nm [7,8]. And the ARPES data show the presence of the Dirac cone with high Fermi velocity of 1.3×10^6 m/s in silicene [6], comparable to that of $1.09 \pm 0.15 \times 10^6$ m/s for graphene [9]. Whereas the DFT [7,8,10] and TB [11] calculations show that similar to graphene, silicene is also a zero-gap semiconductor, and its charge carriers are massless fermions because its π and π^* bands are linearly dispersed (namely Dirac Cone) around the Fermi level (E_f). This would lead to a quite large carrier mobility compared to that of graphene (i.e., 10^4–10^5 cm^2/V s [12–15]).

Meanwhile, new evidences (i.e., atomically resolved STM images [16], K-edge energy loss spectra [17], and ARPES [18]) have proved the synthesis of zigzag-edged silicene nanoribbons (ZSiNRs) on Ag(110) surface with 1.6 nm in width and several hundred nm in length. The first-principles calculations have demonstrated that the nonmagnetic H-terminated ZSiNRs are metals while the H-terminated armchair-edged silicene nanoribbons (ASiNRs) are semiconductors [19,20]. Hence, the ASiNRs can be truncated to a few nm and connected to proper ZSiNR electrodes to form seamless Z-shape semiconducting devices. The quasi-one-dimensional electrode [21–24] can significantly reduce the screening of the gate electric fields effect compared with the bulky metal electrodes [25–27], and the seamless connection between the electrode and scattering region can minimize the series resistances between the channel and the source and drain terminals [28]. Besides, as a silicon counterpart, silicene and its nanoribbons are expected to have the advantage of more easily fitting into the current silicon-based micro/nanoelectronics industry [29].

In this article, we connected ultrashort (4.40–14.51 nm) semiconducting ASiNRs to proper metallic ZSiNRs electrodes to form seamless Z-shape devices, and the ab initio quantum transport calculations are performed. High performance bipolar gate effects with an

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$I_{\rm on}/I_{\rm off}$ ratio of over 10^6 and a subthreshold swing as small as 90 mV/decade are observed in intrinsic ASiNR-based FETs. Inspiringly, the output characteristic exhibits a saturation current, which it is usually absent in carbon-based FETs [30–35].

2 Model and method

We use N_a-ASiNR and N_z-ZSiNR to denote an H-passivated ASiNR and ZSiNR with N_a dimer lines and N_z zigzag chains across the ribbon width, respectively. A vacuum space of 16 Å is placed to avoid interaction between the nanoribbon and its periodic images. Within the framework of DFT, the geometry structures of the infinite N_a-ASiNR ($N_a = 6-11$) and N_z-ZSiNR ($N_z = 4-7$) are relaxed until the maximum atomic force is less than 0.02 eV/Å by using an ultrasoft pseudopotential [36] plane wave basis set as implemented in the CASTEP package [37]. We take a cutoff energy of 260 eV and a $1 \times 1 \times 9$ Monkhorst-Pack [38] k-points grid for the integration of the first Brillouin zone. On the basis of the equilibrium structures, the electronic structures are calculated with a cutoff energy of 400 eV and $1 \times 1 \times 49$ k-points.

The infinite optimized N_a-ASiNRs ($N_a = 6$, 7, 9, and 10) are then truncated to 4.40–14.51 nm and connected to proper optimized ZSiNRs electrodes to form seamless Z-shape devices. We use L to denote the channel length of the N_a-ASiNR-based FET. The transport properties are calculated using the ATK 2008.10 code [39,40], which is based on the DFT coupled with nonequilibrium Green's function (NEGF) method. We use a mesh cut-off energy of 150 Ry and a single-ζ basis set (SZ). The electrode temperature is set as 300 K. The k-points of the electrodes, which are generated by Monkhorst-Pack scheme as well, are set to $1 \times 1 \times 500$. Local density approximation (LDA) of Perdew-Zunger (PZ) form [41] is chosen for the exchange-correlation functional throughout the calculations.

The current is calculated using the Landauer-Büttiker formula [42],

$$I(V_{\rm gate}, V_{\rm bias}) = \frac{2e}{h} \int_{-\infty}^{+\infty} \{T(E, V_{\rm gate}, V_{\rm bias})[f_L(E-\mu_L)] - f_R(E-\mu_R)]\}dE \quad (1)$$

where $T(E, V_{\rm gate}, V_{\rm bias})$ is the transmission probability at a given gate voltage $V_{\rm gate}$ and bias voltage $V_{\rm bias}$, $f_{L/R}$ is the Fermi-Dirac distribution function for the left (L)/right (R) electrode, and μ_L/μ_R is the electrochemical potential of the left (L)/right (R) electrode. In our model, we will take the effect of gate voltage into account by adding a constant shift to the electrostatic potential of the scattering region.

The DFT theory has three shortcomings. One is that it is a ground-state theory, so it can't treat excited states. One is that it doesn't differentiate between the two potentials of occupied (V_{N-1}) and unoccupied states (V_N). And another is that the self-interaction correction is not included and the exchange-correlation potential (V_{XC}) doesn't include nonlocal effects nor energy- and electron density dependencies [43]. Hence, it is noteworthy here that the conventional DFT has a tendency to underestimate the band gap of a semiconductor, and the band gap correction is generally enhanced when the dimension is reduced as a consequence of the enhanced Coulomb interaction effects. For example, the quasi-particle energy correction (GW method) increases the LDA band gap of 10-AGNR (i.e. armchair-edged graphene nanoribbons with 10 dimer lines across the ribbon width) from 1.3 to 3.2 eV [44]. Therefore, the band gaps of the ASiNRs considered in this paper are probably underestimated by more than a half. As a result, the off current and therefore the $I_{\rm on}/I_{\rm off}$ ratios of ASiNR FETs should be underestimated.

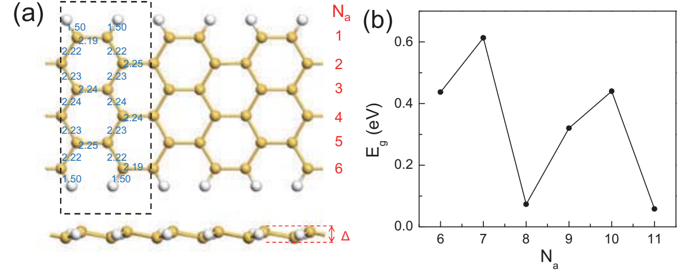

Fig. 1. (Color online) (a) Top and side views of the optimized 6-ASiNR. The primitive cell is denoted by the black rectangle. The relaxed bond lengths in a unit cell are marked. The adjacent Si atoms are slightly buckled with a distance of Δ. Yellow ball: Si; white ball: H. (b) Band gap changes of the N_a-ASiNRs with the width index N_a.

3 Results and discussion

The top and side views of an optimized 6-ASiNR are shown in Figure 1a. The edge diagonal and horizontal Si-Si bonds are slightly shrunk by 0.02 and 0.06 Å from the inner Si-Si bonds of 2.24−2.25 Å (same as the Si-Si bond in silicene), respectively. And the adjacent Si atoms are slightly buckled with a distance of $\Delta = 0.38-0.45$ Å, compared with $\Delta = 0.42$ Å in silicene. These structural parameters are in good agreement with previous works [7,8,19]. The ASiNRs are semiconductors with direct band gaps located at the Γ points, while the ZSiNRs are metals. We give the band gaps of the N_a-ASiNR ($N_a = 6-11$) in Figure 2b. These band gaps belong to three branches with widths $N_a = 3k$, $3k+1$, $3k+2$ (k is an integer) as Family I, II, and III, respectively, and the band gap of each family deceases with the increasing width. The band gaps of the 6-, 7-, 9-, and 10-ASiNRs are 0.44, 0.61, 0.32, and 0.44 eV, respectively. Our results are consistent with the previous work [19].

A gated two-probe model constructed by an optimized truncated 6-ASiNR connected to the 4-ZSiNR electrodes is shown in Figure 2a The calculated transfer characteristics at $V_{\rm bias} = 0.02$ V for all the calculated FETs with different channel lengths are presented in Figures 2b−2d.

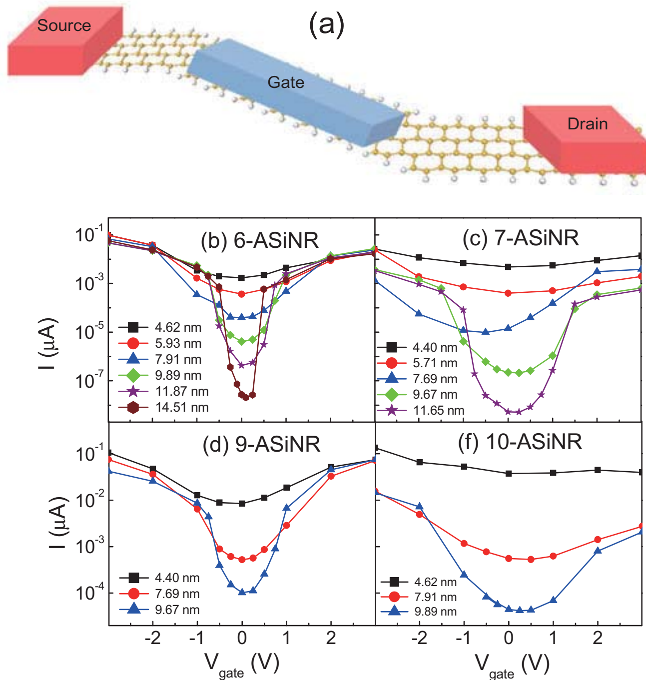

Fig. 2. (Color online) (a) A gated two-probe model constructed by an optimized 6-ASiNR connected to the 4-ZSiNR electrodes. The channel length is 4.62 nm. Yellow ball: Si; white ball: H. (b)–(d) Calculated transfer characteristics at $V_{\rm bias} = 0.02$ V of the N_a-ASiNR ($N_a = 6$, 7, 9, and 10) FETs as a function of the channel length.

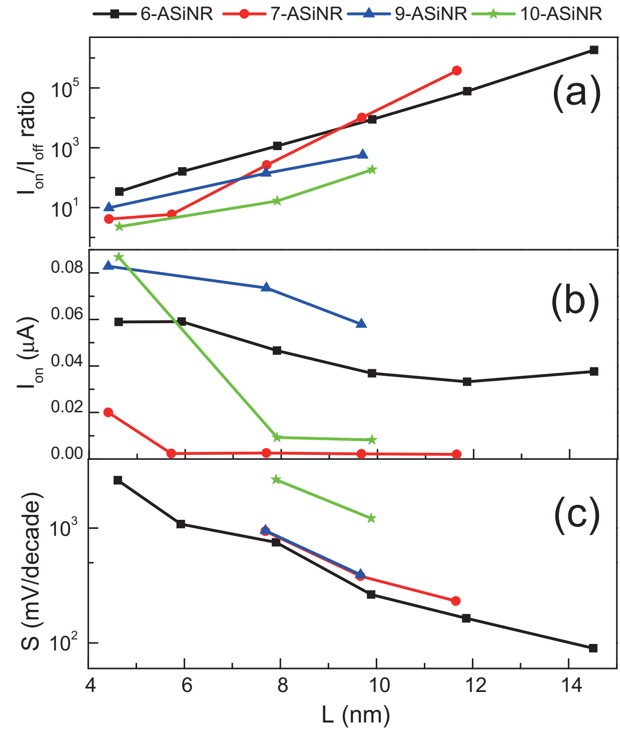

Fig. 3. (Color online) (a) $I_{\rm on}/I_{\rm off}$ ratios, (b) on-state currents, and (c) subthreshold swings (S) of the N_a-ASiNR ($N_a = 6$, 7, 9, and 10) FETs at $V_{\rm bias} = 0.02$ V as a function of the channel length (L).

Perfect bipolar gate effects are observed for the 6- and 9-ASiNR FETs, while the current valleys move slightly to a positive gate voltage for the 7- and 10-ASiNR FETs expect for the 7-ASiNR ($L = 7.69$ nm) FET with the current valley at a negative gate voltage. The value of $V_{\rm gate}$ at which the FET is just on the verge of switching on is the threshold voltage, $V_{\rm th}$. The $V_{\rm th}$ usually happens at $V_{\rm gate} \approx \pm 1$ V for the shortest effective ASiNR FETs ($I_{\rm on}/I_{\rm off} \geqslant 10$), and it gradually move to a smaller absolute value with the increasing L.

The $I_{\rm on}/I_{\rm off}$ ratios ($V_{\rm bias} = 0.02$ V) of the checked AGNRs as a function of L are shown in Figure 3a. Because the I-$V_{\rm gate}$ curves are often slightly asymmetric, the value of $I_{\rm on}$ is averaged over the $I_{\rm on}$ on the positive and negative $V_{\rm gate}$. The $I_{\rm on}/I_{\rm off}$ ratios are monotonously enhanced with L for a given ASiNR FET. This tendency has also been obtained theoretically in bipolar Z-shape armchair-edged graphene nanoribbons (AGNRs) FETs [35] and n-type silicon nanowires (SiNWs) FETs [45]. The increased $I_{\rm on}/I_{\rm off}$ ratios with L in the ultrashort ASiNR-based FETs originate from the fact that the off-state currents drop more rapidly with L than the on-state current (see Figs. 2b–2d) because the tunneling probability of the off-state current decreases rapidly with L. At a given L, the $I_{\rm on}/I_{\rm off}$ ratio decreases with the increasing nanoribbon width for the ASiNRs belong to the same family. The $I_{\rm on}/I_{\rm off}$ ratios of the ASiNR FETs belong to Family I are smaller than those of the ASiNR FETs with similar L belong to Family II with same k at a shorter L. For example, the $I_{\rm on}/I_{\rm off}$ ratio of the 7-ASiNR FET is smaller than that of the 6-ASiNR FET with similar L when L is shorter than ~10.0 nm. The $I_{\rm on}/I_{\rm off}$ ratios of the 6-ASiNR FETs with $L \geqslant 7.91$ nm and the 7-ASiNR FETs with $L \geqslant 9.67$ nm are over 10^3, and especially the $I_{\rm on}/I_{\rm off}$ ratio is up to over 10^6 in the 6-ASiNR ($L = 14.51$ nm) FET. The $I_{\rm on}/I_{\rm off}$ ratios of the 9-ASiNR ($L = 9.67$ nm) and 10-ASiNR ($L = 9.89$ nm) FETs are over 10^2. We expect the $I_{\rm on}/I_{\rm off}$ ratios of the 9- and 10-ASiNR FETs will be over 10^3 when the channel lengths are larger than 12 nm. The bipolar 10-AGNR FET with $L = 5.91$ nm and the n-type SiNW FET with $L = 7$ nm have theoretical $I_{\rm on}/I_{\rm off}$ ratios of 2×10^3 at $V_{\rm bias} = 0.02$ V [35] and ~10^4 at $V_{\rm bias} = 0.5$ V [45], respectively.

The on-state current determines the FET switching speed, whereas the off-state current determines the passive power consumed by a logic gate (e.g., an inverter). A high-speed low-power device should possess both high $I_{\rm on}/I_{\rm off}$ ratio and $I_{\rm on}$. The $I_{\rm on}$ values ($V_{\rm bias} = 0.02$ V) of all ASiNR FETs are shown in Figure 3b as a function of L. The on-currents for a given ASiNR FET are generally decreased rapidly at first and then are saturated with increasing L. For example, the $I_{\rm on}$ values of the 6-ASiNR FETs generally decrease from 5.90×10^{-2} to 3.69×10^{-2} μA when L increases from 4.62 to 9.89 nm, and then it is nearly unchanged until L increases to 11.45 nm. We find that the $I_{\rm on}$ values increase in the orders of 7- < 10- < 6- < 9-ASiNR FETs with similar L expect for

10-ASiNR(4.62 nm). For example, the $I_{\rm on}$ values of the 6-ASiNR ($L = 9.89$ nm), 7-ASiNR ($L = 9.67$ nm), 9-ASiNR ($L = 9.67$ nm), and 10-ASiNR ($L = 9.89$ nm) FETs are 3.69×10^{-2}, 2.12×10^{-3}, 5.79×10^{-2}, and 8.23×10^{-3} μA, respectively. The theoretical $I_{\rm on}$ values of the bipolar 10-AGNR FET with $L = 5.91$ nm and the n-type SiNW FET with $L = 7$ nm are about 0.7 μA at $V_{\rm bias} = 0.02$ V [35] and about 3 μA at $V_{\rm bias} = 0.5$ V [45], respectively, which are a few tens and a few times larger then the $I_{\rm on}$ values of our ASiNR FETs.

The subthreshold swing (S) is also an important parameter of FETs. It determines how effectively the transistor can be turned off by changing the gate voltage. The smaller the S, the sharper of the on-off switching of a transistor. It has a theoretical best value of $S = (k_B T/q)\ln(10)$ (k_B and q are the Boltzmann constant and the charge of the carriers, respectively), corresponding to numerical value of 60 mV/decade at $T = 300$ K. The S values ($V_{\rm bias} = 0.02$ V) of all the ASiNR FETs with an $I_{\rm on}/I_{\rm off}$ ratio >10 are shown in Figure 3c as a function of L (S here is defined as averaged $dV_{\rm gate}/d(\log I)$ over the value in the positive and negative $V_{\rm gate}$ related to the sub-threshold region). The subthreshold swings monotonously decrease with increasing L for a given ASiNR FET. For example, the S values of the 6-ASiNR FETs decrease from 2616 to 90 mV/decade when L increases from 4.62 to 14.51 nm. Whereas, the theoretical S values of the bipolar 10-AGNR FETs decrease from 2250 to 60 mV/decade when L increases from 1.69 to 6.76 nm [35] and the theoretical S values of the n-type SiNW FETs decrease from 132 to 65 mV/decade when L increases from 7 to 25 nm [45]. At a given L, the S increases with the increasing nanoribbon width for the ASiNRs belong to the same family. In specific, the S values decrease in the orders of 10- $>$ 9- $\approx$ 7- $>$ 6-ASiNR FETs with similar L. For example, the S values of 6-ASiNR ($L = 9.89$ nm), 7-ASiNR ($L = 9.67$ nm), 9-ASiNR ($L = 9.67$ nm), and 10-ASiNR ($L = 9.89$ nm) are 264, 381, 394, and 1217 mV/decade, respectively.

The transmission eigenchannels and at the Γ points at E_f for the off- ($V_{\rm gate} = 0.0$ V) and on-states ($V_{\rm gate} = -3.0$ V) of the 6-ASiNR ($L = 4.62$ nm) FET are given in Figures 4a and 4b, respectively. The transmission eigenvalue of the on-state is 1.03×10^{-2} and it decreases one order of magnitude in the off-state to a value of 1.05×10^{-3}. This implies that more electrons can reach the right lead in the on-state as can be seen from the wavefunctions in the figure.

The calculated output characteristic of the 6-ASiNR ($L = 9.89$ nm) FET is given in Figure 5a. This is a typical output characteristic of a FET. Namely, the currents are at first increase linearly ($V_{\rm bias} < 0.1$ V) and then become a constant ($V_{\rm bias} \geqslant 0.1$ V) with the increasing bias voltage at the above-threshold region ($V_{\rm gate} \geqslant V_{\rm th} \approx -1$ V). The saturated output characteristic is an advantage with respect to device speed. Whereas the output characteristics of many carbon-based (e.g., graphene [32–34], graphene nanoribbons [35], carbon nanotubes [31], and organic single-molecule [30] FETs either show a linear shape without any saturation or only weak saturation. The saturated output characteristic of the ASiNR-based FETs is a prominent advantage to carbon-based FETs. As to the SiNW-based FETs, both the output current saturated [46,47] and unsaturated characters are obtained [48–50].

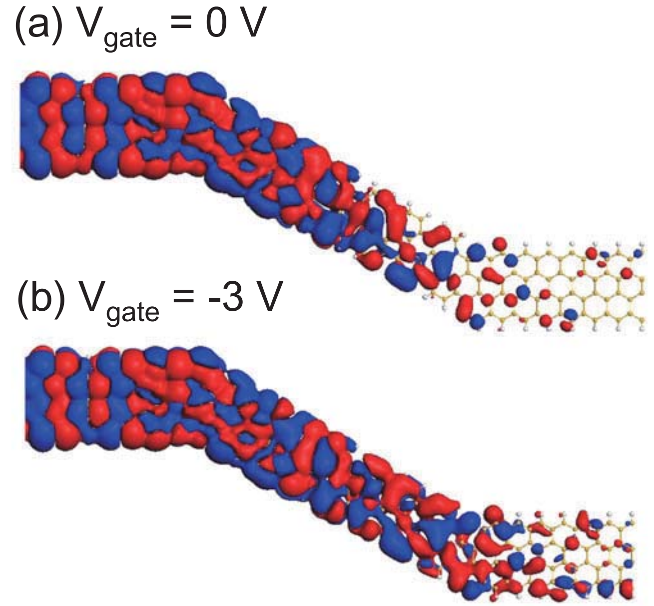

Fig. 4. (Color online) (a, b) Transmission eigenchannels at the Γ points and at the Fermi level of the 6-ASiNR ($L = 4.62$ nm) FET at a gate voltage of 0 (a) and 3 V (b). The isovalue is 0.001 a.u. Red and blue are used to indicate the positive and negative signs of the wavefunctions, respectively. Yellow ball: Si; white ball: H.

We finally investigate whether an n- and p-type FET can be obtained via substituting two edge Si atoms with phosphorus (P) and boron (B) atoms, respectively. It corresponds to a dopant concentration of $\sim 1.68 \times 10^{13}/{\rm cm}^2$. The resulting transfer characteristics of the pure and doped 6-ASiNR ($L = 9.89$ nm) FETs are shown in Figure 5b. The off-state moves from $V_{\rm gate} = 0.0$ to -7.0 and 4.0 V for P and B doping, respectively, suggestive of a transition from bipolar behavior to n- and p-type ones, respectively. After doping, the leakage currents of the n- and p-type FETs increase from 4.10×10^{-6} to 2.67×10^{-4} and 1.31×10^{-4} μA, respectively, while the on-state currents at the positive and negative gate voltage increase from 2.74×10^{-2} to 1.57×10^{-1} μA and from 4.64×10^{-2} to 2.34×10^{-1} μA, respectively. Thus the $I_{\rm on}/I_{\rm off}$ ratios of n- and p-type FETs decrease by about 15 and 5 times from 8.99×10^3 to 5.89×10^2 and 1.78×10^3, respectively. Subthreshold swings at the positive and negative sub-threshold region of 1814 and 1198 mV/decade are obtained in the n- and p-type FETs, respectively, larger than a value of 264 mV/decade in the undoped one. The decrease in the $I_{\rm on}/I_{\rm off}$ ratio is also predicted in the Z-shape AGNR FET after N doping [35] and the functionalized metallic single-walled carbon nanotube FET after K doping [28].

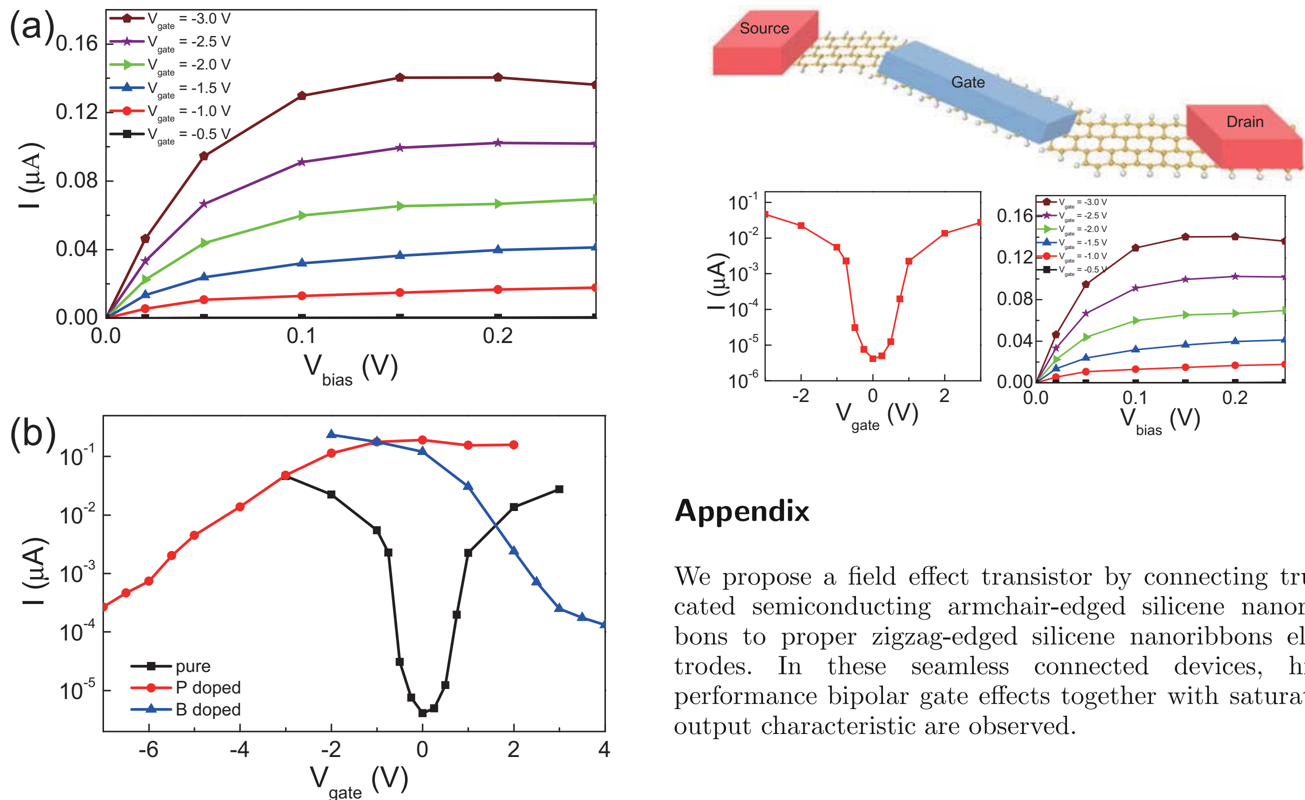

Fig. 5. (Color online) (a) Calculated output characteristic of the 6-ASiNR ($L = 9.89$ nm) FET. The gate voltage varies from -0.5 to -3.0 V in a step of 0.5 V. (b) Calculated transfer characteristics ($V_{\text{bias}} = 0.02$ V) of the 6-ASiNR ($L = 9.89$ nm) FETs with phosphorus (P) and boron (B) atom doping, respectively.

4 Conclusion

In conclusion, we have predicted saturated and high performance field effect transistors from armchair-edged silicene nanoribbons by using ab initio quantum transport calculations. The intrinsic ASiNR-based FETs exhibit high performances bipolar gate effect with an $I_{\text{on}}/I_{\text{off}}$ ratio of over 10^6 and a subthreshold swing as small as 90 mV/decade. The overall performance can be further enhanced by increasing the channel length. Inspiringly, the output characteristic shows a saturation behavior, while it is usually absent in carbon-based FETs. These advantage characters make the ASiNR-based FETs promising in the future nanoelectronics.

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Appendix

We propose a field effect transistor by connecting truncated semiconducting armchair-edged silicene nanoribbons to proper zigzag-edged silicene nanoribbons electrodes. In these seamless connected devices, high performance bipolar gate effects together with saturated output characteristic are observed.

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